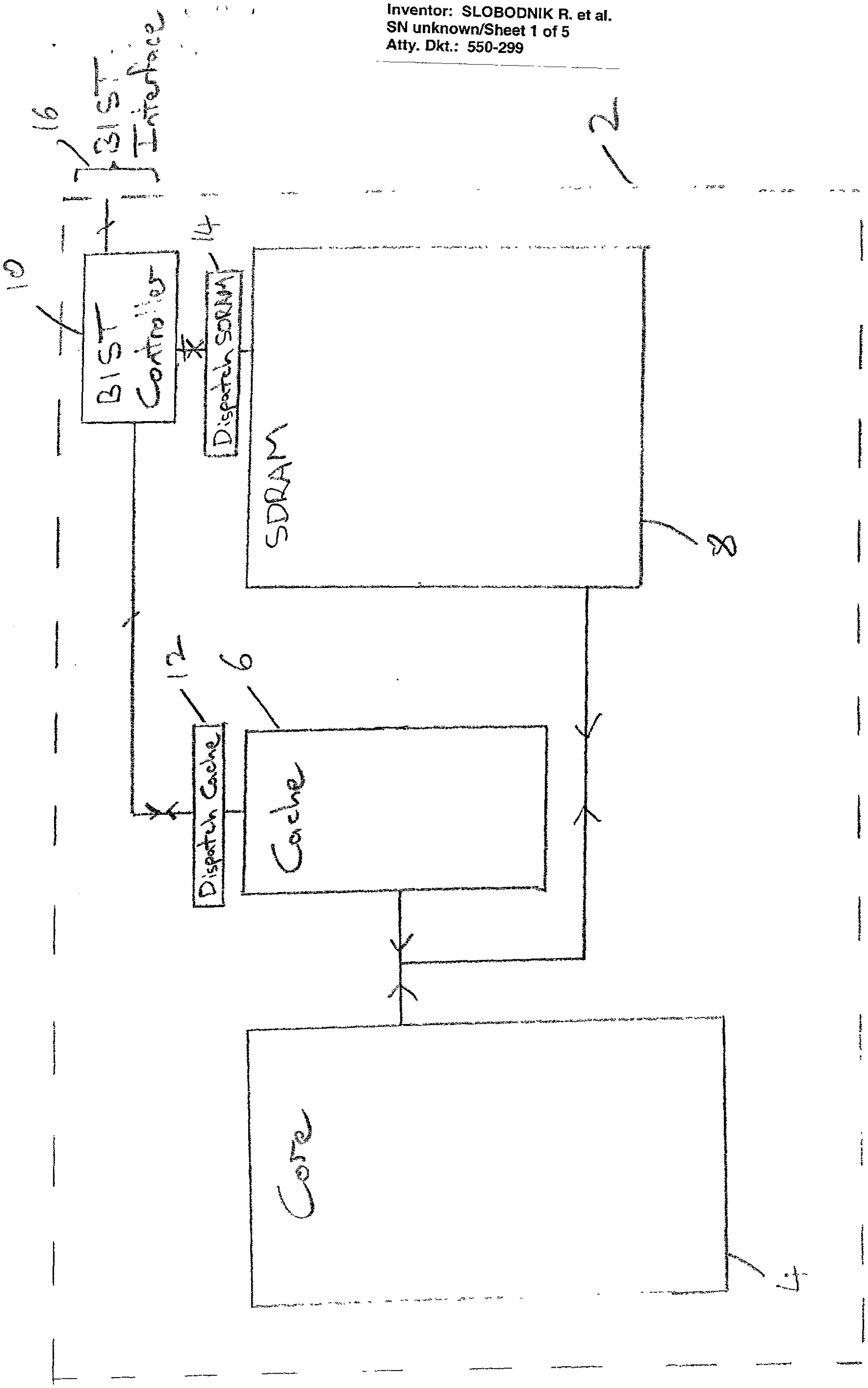

BIST Interface
16
2
10
BIST Controller
14
Dispatch SDRAM
SDRAM
8
12
6
Dispatch Cache
Cache
Core
4

Fig. 1

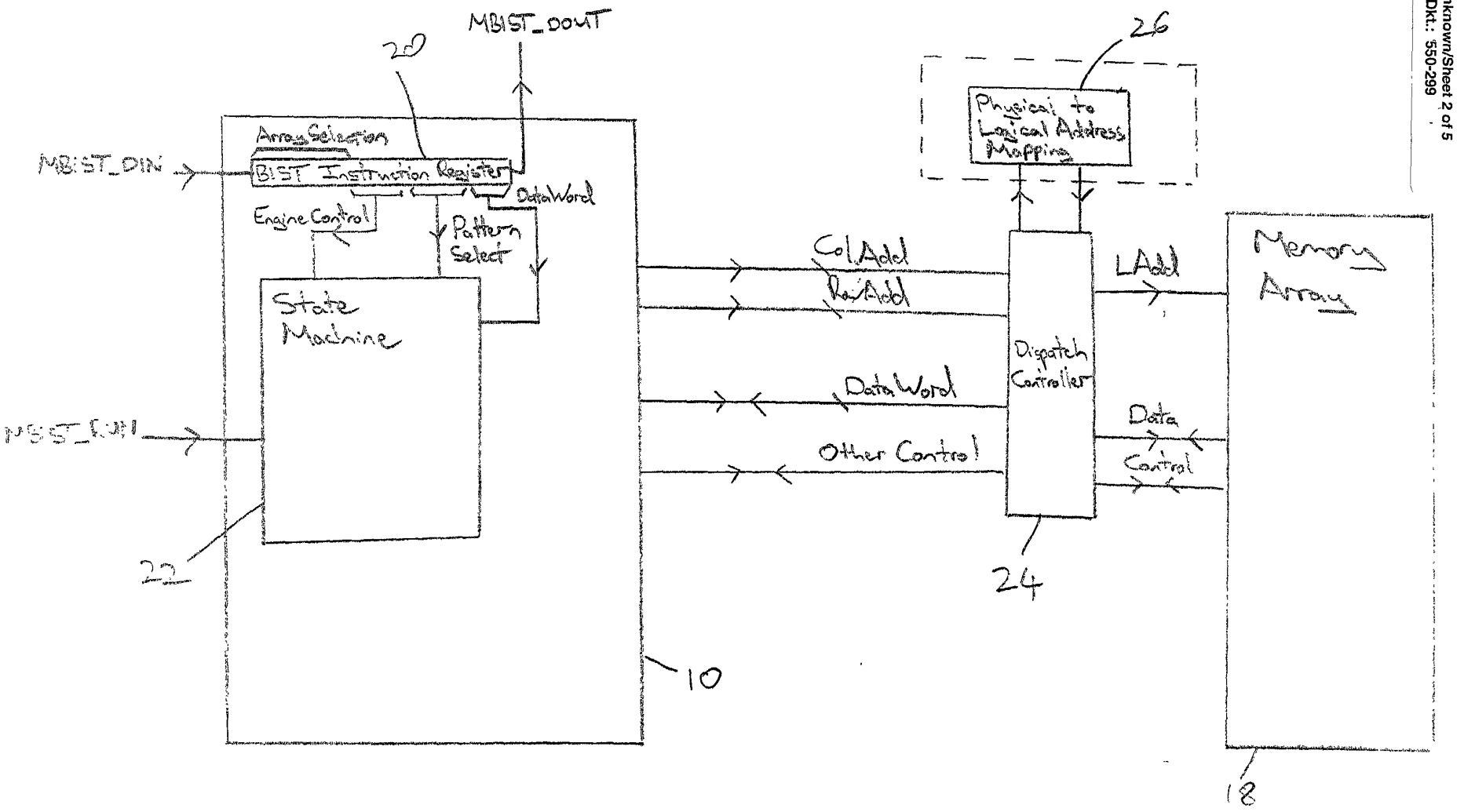

MBIST_DOUT
20
26
Physical to Logical Address Mapping
Array Selection
MBIST_DIN
BIST Instruction Register
DataWord
Engine Control
Pattern Select
State Machine
ColAdd
RowAdd
LAdd
Memory Array
Dispatch Controller
DataWord
Data
Other Control
Control
MBIST_EN
22
24
10
18

Fig. 2

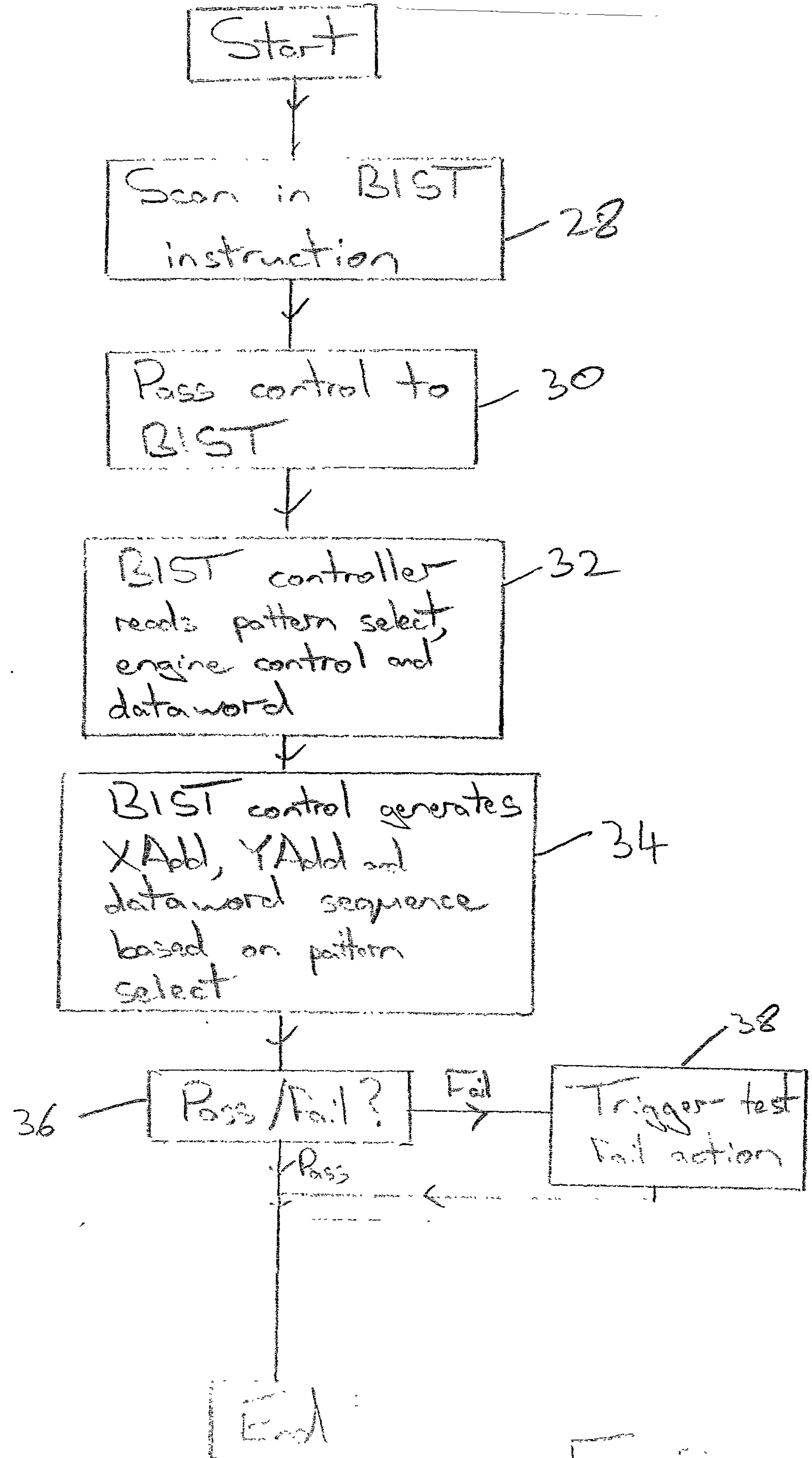

Start
Scan in BIST instruction
28
Pass control to BIST
30
BIST controller reads pattern select, engine control and dataword
32
BIST control generates XAdd, YAdd and dataword sequence based on pattern select
34
36
Pass/Fail?
Fail
Trigger test Fail action
38
Pass
End

Fig. 3

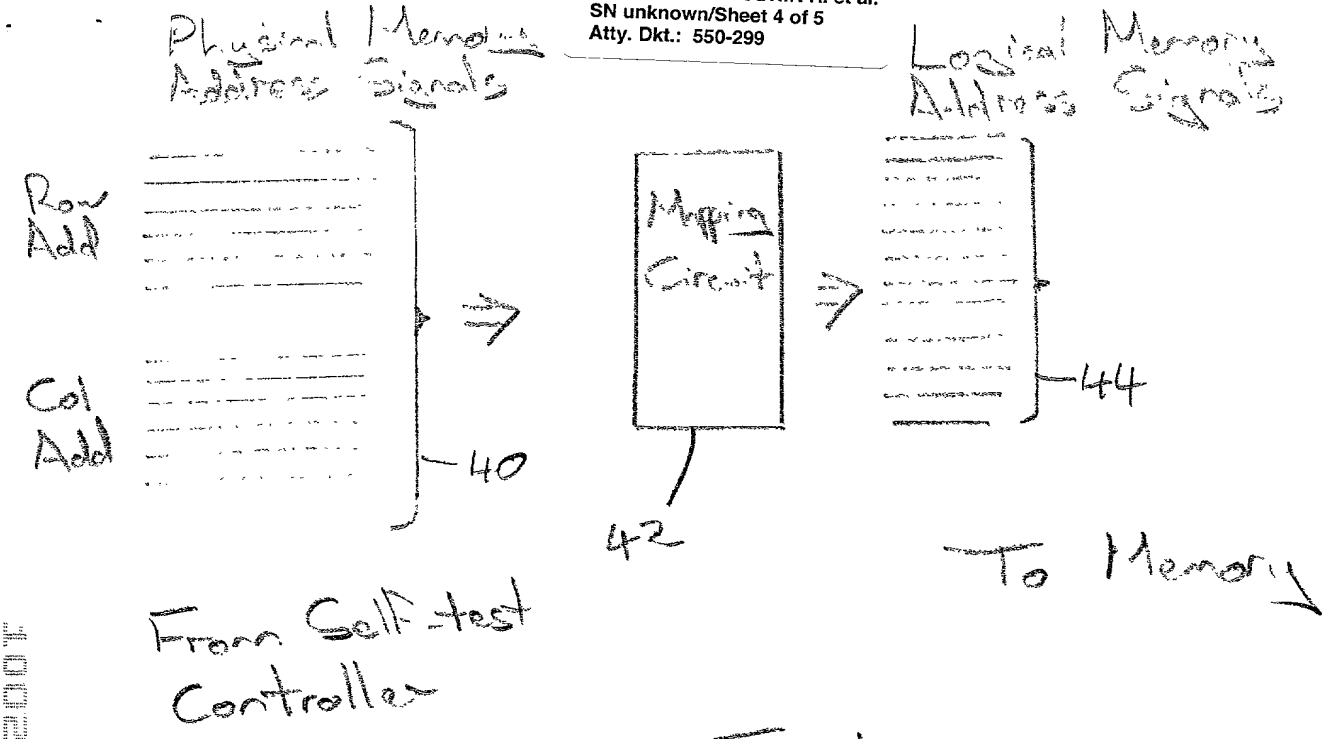
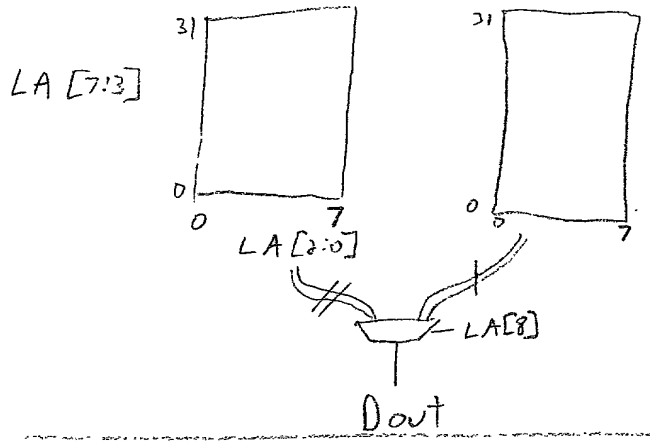

Physical Memory Address Signals
Logical Memory Address Signals
Row Add
Col Add
40
Mapping Circuit
42
44
From Self-test Controller
To Memory

Fig. 4

LA [8:0] when implemented has 32 rows, 8 cols, 1 block select



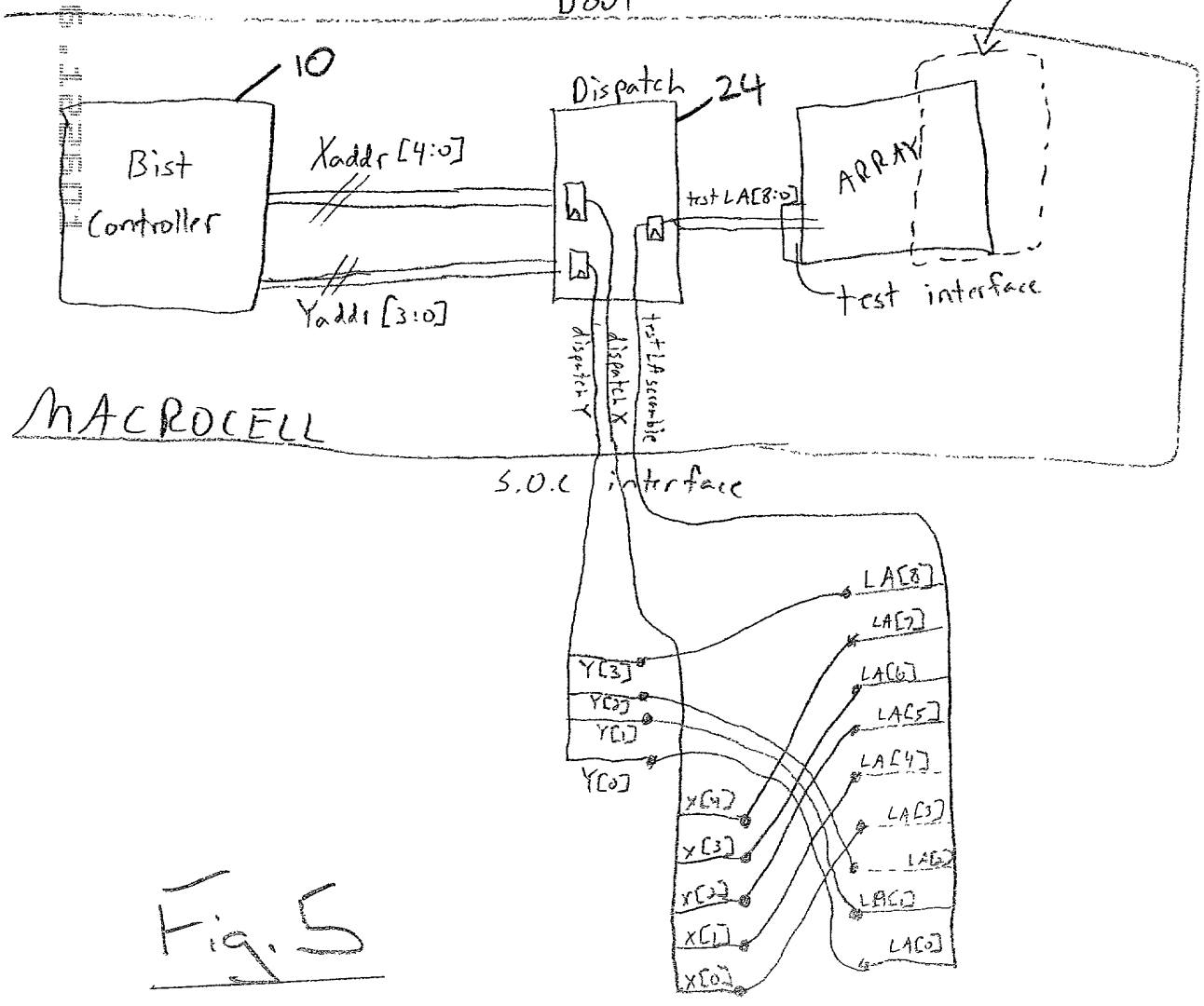


Fig. 5